CLAIMS

1. Apparatus for use in a computer system comprising:

a bus architecture;

a plurality of modules connected to the bus architecture, each module being assigned an address range in a memory map of the apparatus;

each module comprising:

reception means for receiving and storing availability data indicative of the availability of modules;

transaction request means for producing a transaction request including target address data indicating a target location in the memory map for the transaction;

decoding means for decoding the target address data to produce identity data relating to a target module, the target module being assigned an address range in the memory map which includes the target address data;

comparison means for analysing the stored availability data corresponding to the target module identified by the identity data; and.

transaction means, responsive to the comparison means, for terminating the transaction request if the analysed availability data indicates that the target module is unavailable.

2. Apparatus as claimed in claim 1, comprising a control means for controlling access to the bus architecture by the modules and wherein the transaction request to the control means is operable to forward the transaction request to the control means, if the analysed availability data indicates that the target module is available.

3. A computer system comprising apparatus as claimed

in claim 1.

4. An integrated circuit comprising apparatus as claimed in claim 1.